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Research Article

A Novel Approach To Design A Multiplexer Circuit With Reversible Logic Using PRTM Gate

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ABSTRACT- In the recent years, the reversible logic has developed as one of the promising research areas. Its various applications are low power CMOS, quantum computing, cryptography, optical computing, DMA graphics, nanotechnology, quantum Dot automata for mobile, communication and digital signal processing etc. It is considered the fastest rising technology for digital circuit design. Its goal is to design low-power loss digital circuits. In reversible logic gate there is no feedback.This paper offerings the execution of multiplexer using new reversible gate (PRTM).

Keywords: - Reversible gate, Logic gate, Low power

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INTRODUCTION – Research on reversibility was started in 1980's. 1994 Shor did a remarkable research work in creating algorithm using reversibility for factorizing with large number with better efficiency when compared to the classical theory. Today's computer erase a bit of information every time they perform a logic operation it is irreversible and dissipation of energy is also increased. But if we reduce the energy dissipation by each logic operation and in this operation if it do not erase information then it is called reversible logic operation.

For reversibility two conditions must be satisfied-

- Number of input lines must be equal to the number of output lines.
- Feedback is not allowed.
- Fanout must be one.

REVERSIBLE LOGIC GATES –

A) **TOFFOLI GATE -** This gate was invented by TOMMSO TOFFOLI and is a universal reversible logic gate. It is a 3*3 gate. If the first two bits are set, it inverts the third bit, otherwise all bits remain the same. Its quantum cost is 5. It is also called CCNOT 'or' controlled-controlled not gate.

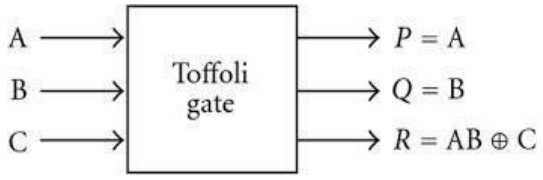

FIG 1: Block diagram of Toffoli gate

B) **PRTM GATE** – PRTM is a 10:10 reversible logic gate which follows the basic characteristics of the

reversible gates. The block diagram of PRTM gate is given below –

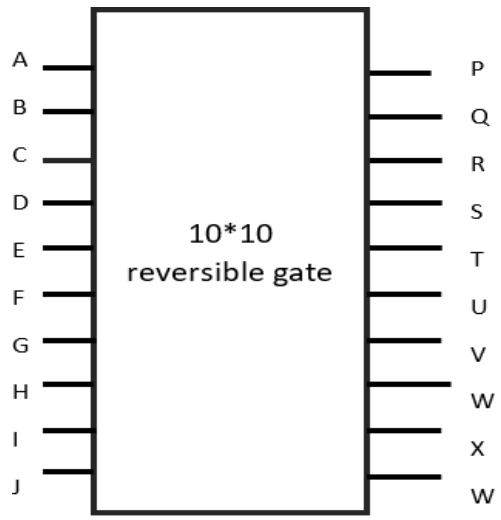

FIGURE 2

P = $\bar{A}B \oplus$ AC , Q = $\bar{A}B \oplus$ AC $\oplus$ D, R = $\bar{E}F \oplus$ EG, S = D, T = E, U = $(F + G) \oplus$ H, V = $H \oplus$ I $\oplus$ J, W = $IJ \oplus$ A, X = $G \oplus$ H, Y= $(\bar{A} + J) \oplus$ F

MULTIPLEXER CIRCUIT – Multiplexer considered as mainly data selector circuit. The selection is directed by a distinct set of digital inputs recognized as select lines. To propose a multiplexer circuit by means of reversible logic gate a smaller number of conditions for reversible circuit designing has to be followed.

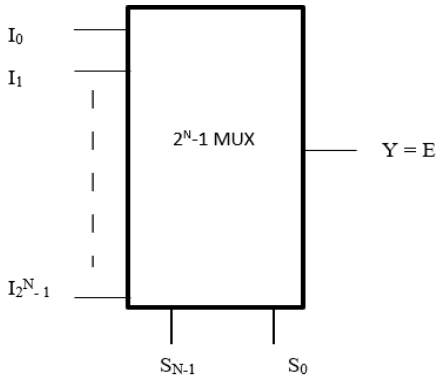

FIG 3:

$Y = E = I_0(S_{N-1} - -\bar{S}_1.\bar{S}_0) + I_1(\bar{S}_{N-1}$ -------- $\bar{S}_1.\bar{S}_0) + - - I^N_{2N-1}(S_{N-1}$---$S_1S_0)$

Here input signals are I_0, I_1, I_2 --- I_{2n-1}, selection lines are S_0, S_1 --- S_{N-1} and output Y.

16: 1 MULTIPLEXER -

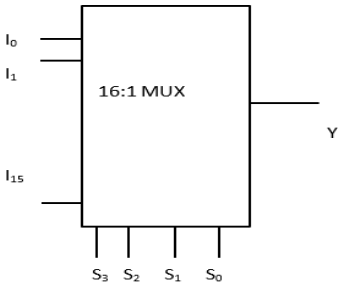

FIG:4

Design of 16:1 multiplexer using PRTM gate and Toffoli gate -

Here we introduced the 16:1 multiplexer circuit using PRTM and Toffoli gate. Designing of 16:1 multiplexer is described-

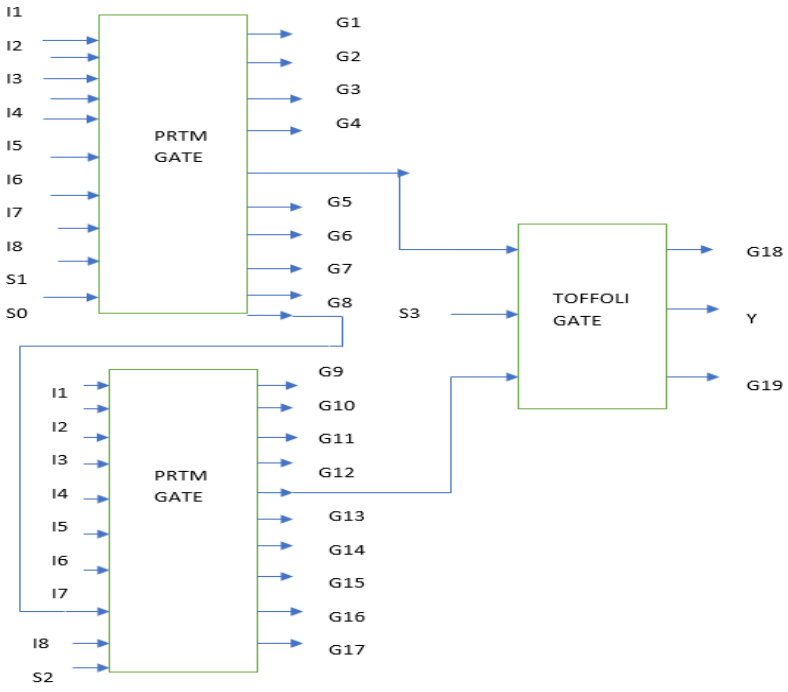

FIG:5

COMPARISON TABLE -

DESIGN	***TOTAL REVERSIBLE GATES***	***TOTAL GARBAGE OUTPUT***	***QUANTUM COST***
Existing design(FRG)	**Unknown**	**Unknown**	**75**
Design2(SAM)	**15**	**20**	**60**
Design3(MFRG)	**15**	**19**	**60**
Proposed design (PRTM)	**03**	**19**	**59**

COMPARISON CHART -

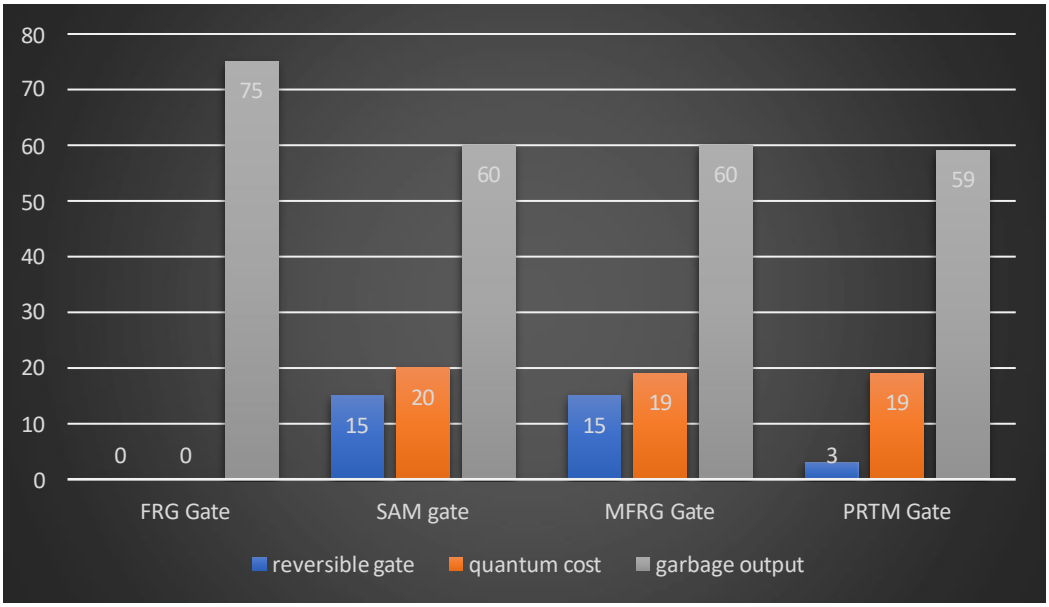

FIG: 6

SIMULATION GRAPH

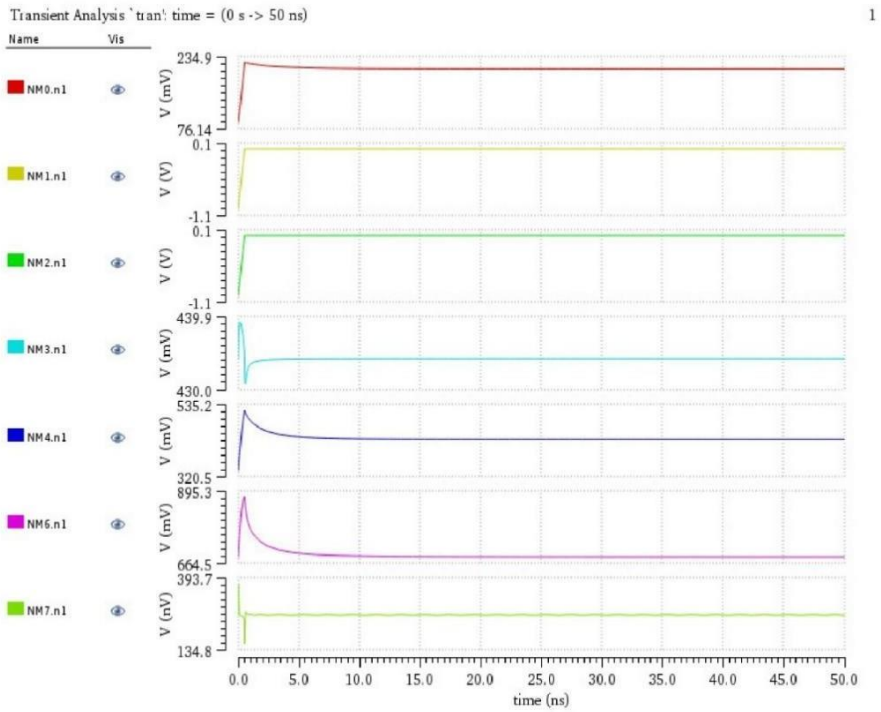

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FIG: 7

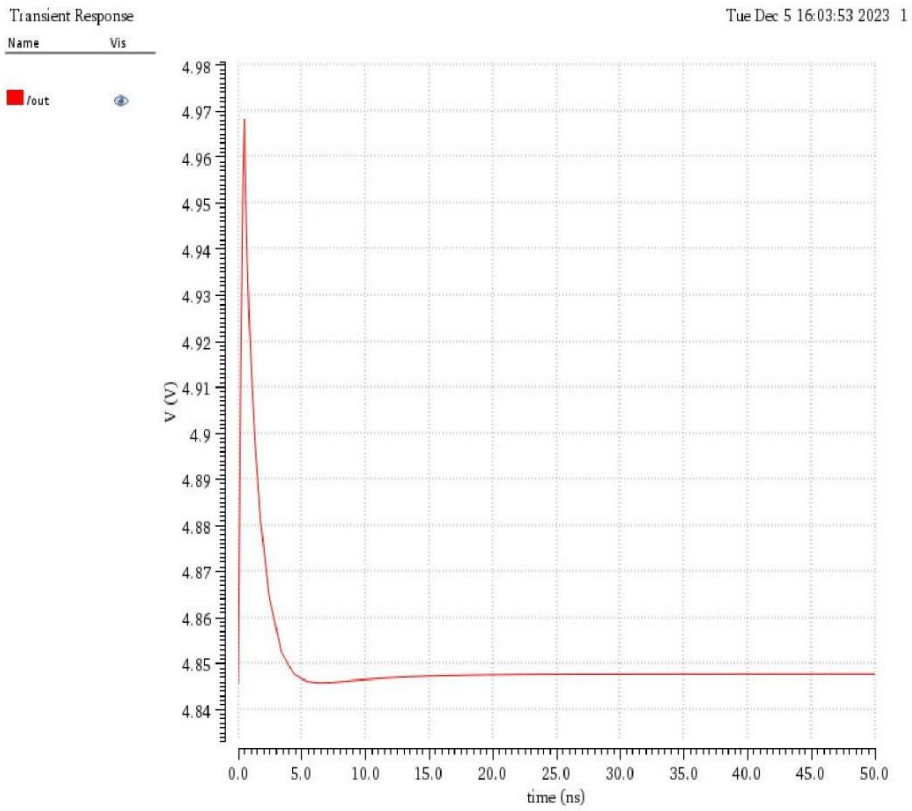

FIG: 8

PROBLEM – Given $X_1 = A \oplus B \oplus k$

$$Y_1 = \bar{A}B \oplus Ak$$
$$Z_1 = \bar{A}k \oplus AB$$

Design Half Adder and Half Subtractor circuit working together.

SOLUTION – When we put k= 0 then we get the equation of half adder and half subtractor, therefore equation

$$X_1 = A \oplus B$$
$$Y_1 = \bar{A}B$$
$$Z_1 = AB$$

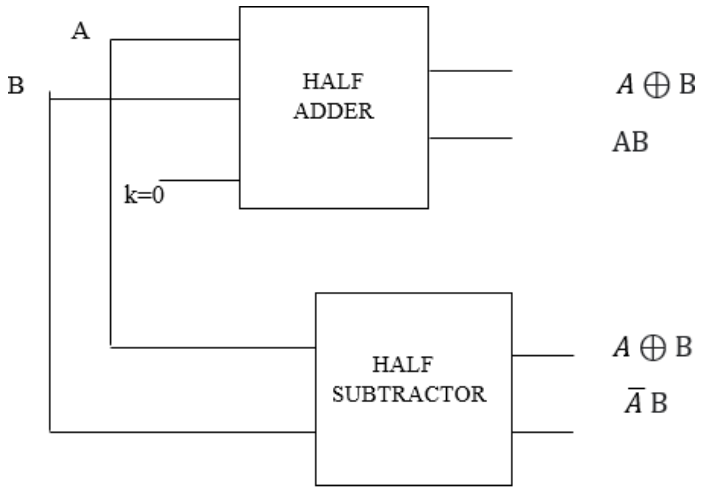

FIG: 9

CONCLUSION AND FUTURE SCOPE-

We have designed a 16:1 multiplexer using reversible logic gates. The proposed circuit for 16:1 multiplexer has better performance as compared to the existing one in terms of total number of reversible gates as well as garbage outputs. This design can be further expanded to reduced the garbage outputs 'or' to accomplish the reversible circuits for various functions and devices. We can minimize the garbage outputs and convert the circuit into more efficient.

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